

VZ3 Block Diagram

PCB HDI Stackups

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND1
LAYER 8 : BOT

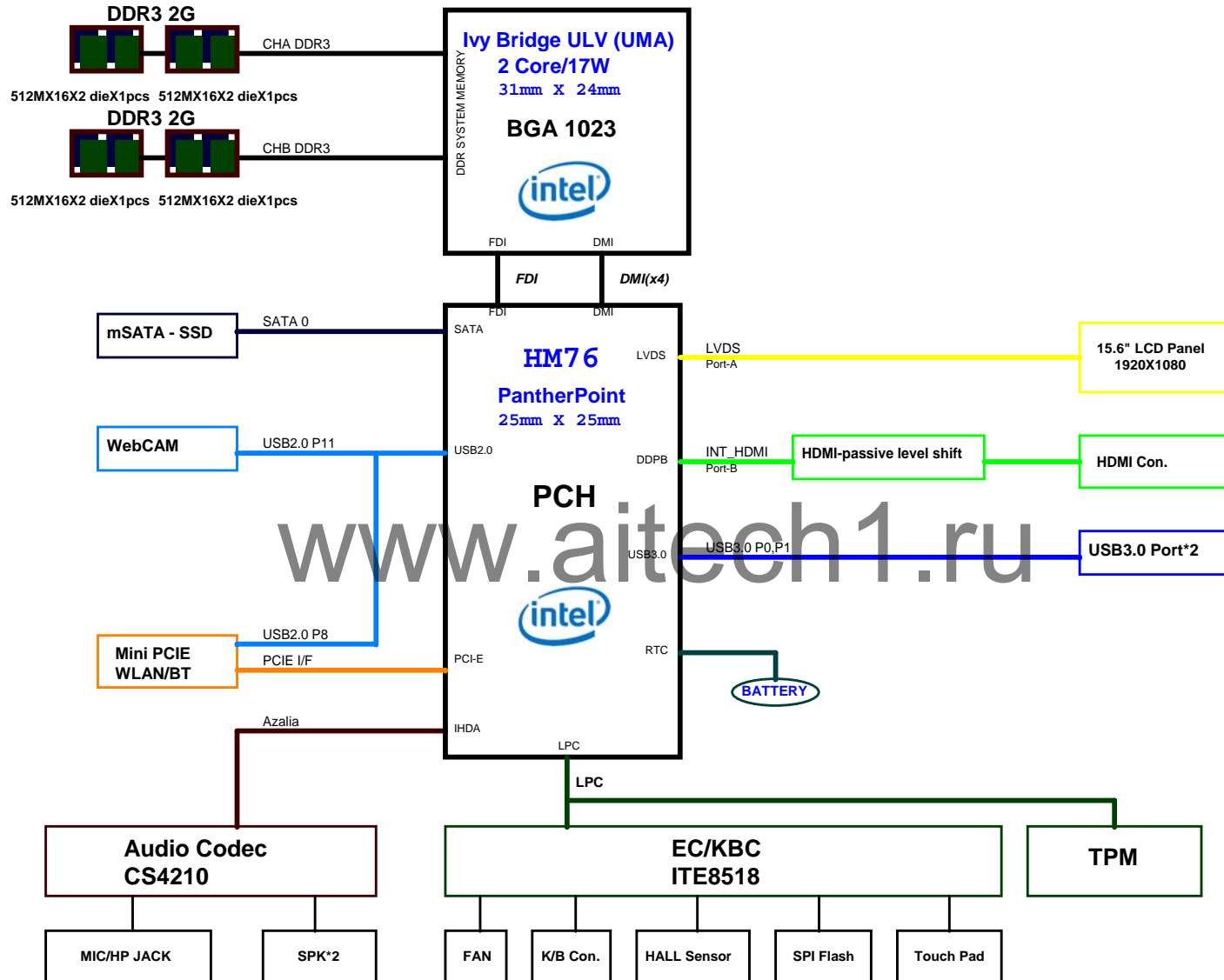


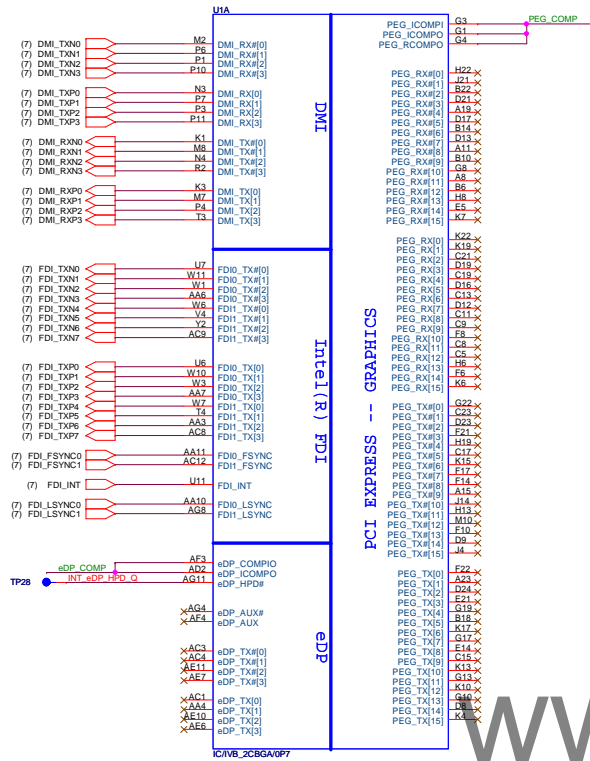
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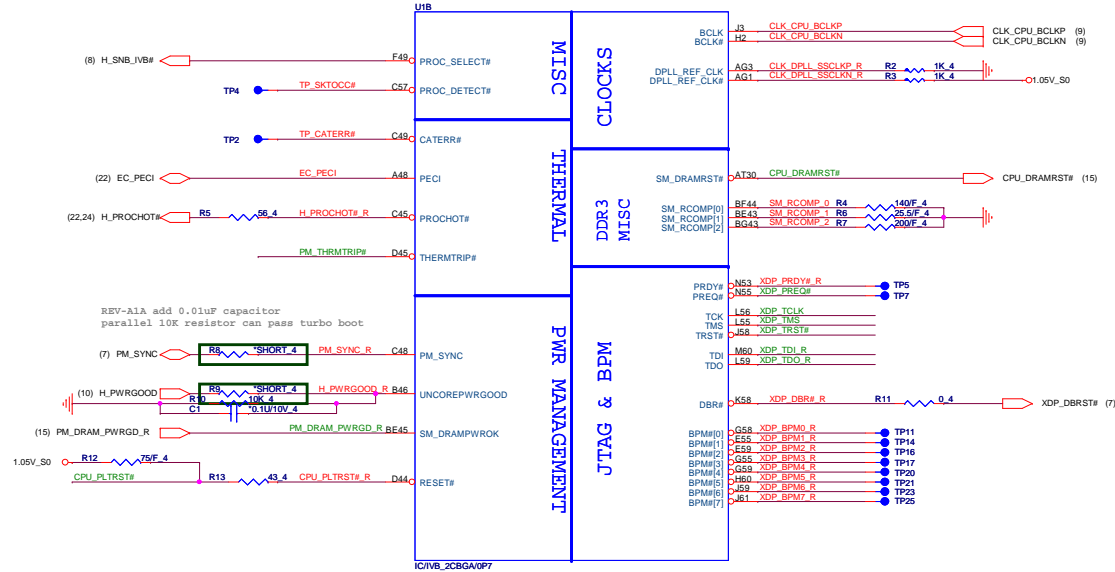
Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
VCCRTC	3V	ON	ON	ON	ON	ON	
VIN	19.5V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
12V_S5	12V	ON	ON	ON	OFF	OFF	S5_ON
5V_S5	5V	ON	ON	ON	OFF	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	OFF	OFF	S5_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	S3_ON
1.5V_CPU	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON1
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON1
3V_S0	3V	ON	OFF	OFF	OFF	OFF	S0_ON1
1.8V_SFR	1.8V	ON	OFF	OFF	OFF	OFF	S0_ON2
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON2
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	S0_ON2
VCCSA	0.65~0.9V	ON	OFF	OFF	OFF	OFF	S0_ON2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON2
VCC_GFX	By VID	ON	OFF	OFF	OFF	OFF	Vron
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	Vron

Ivy Bridge Processor (DMI,PEG,FDI)

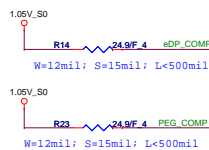


Ivy Bridge Processor (CLK,MISC,JTAG)

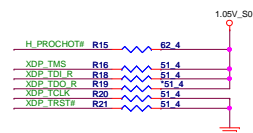


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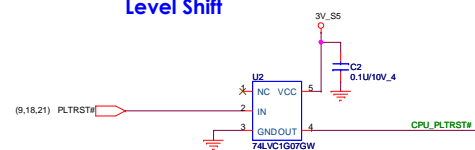
DP & PEG Compensation



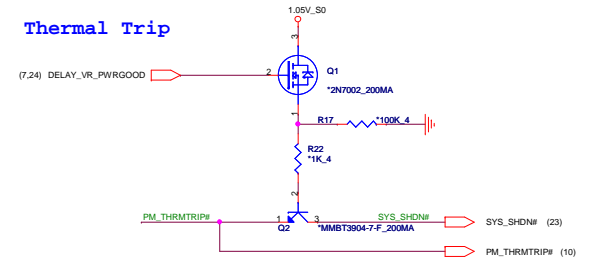
Processor pull-up



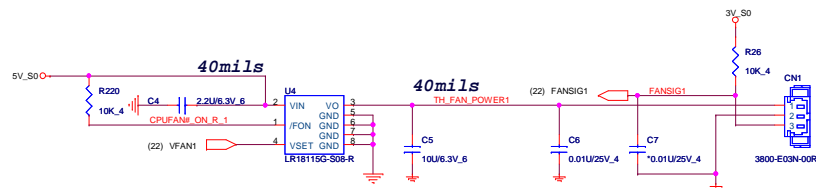
Level Shift



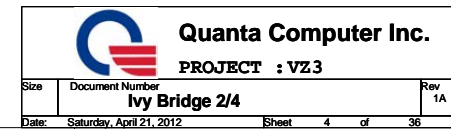
Thermal Trip

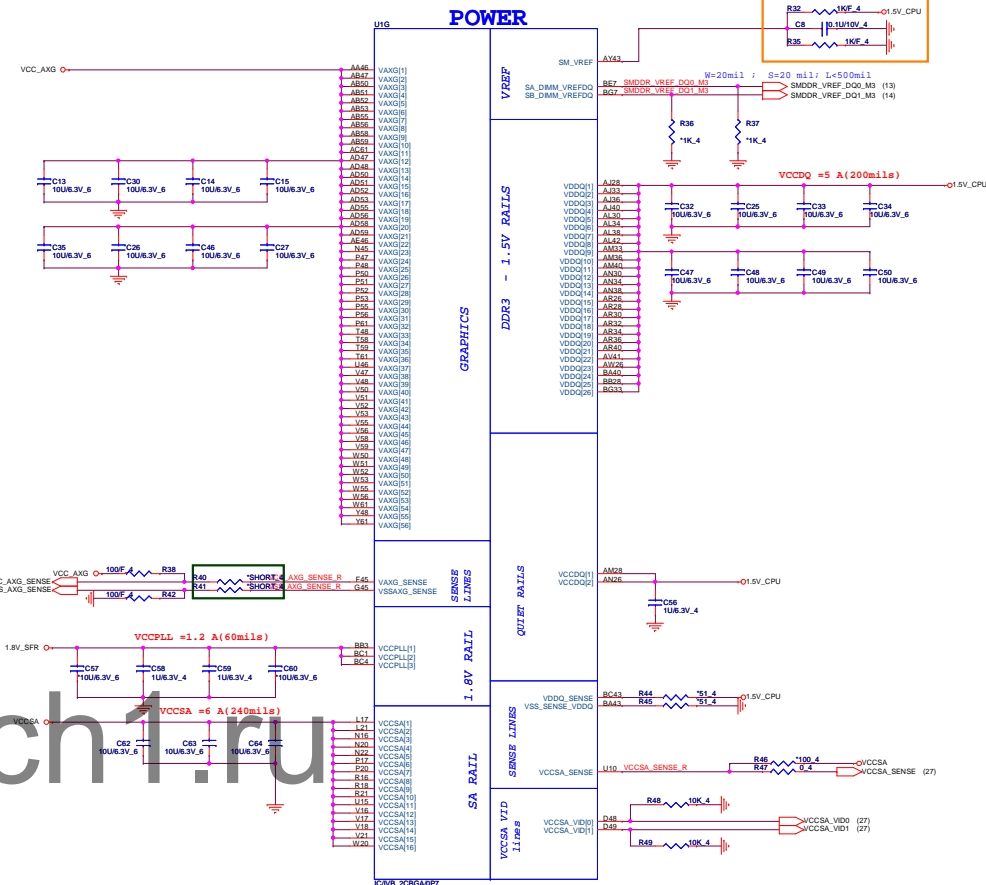
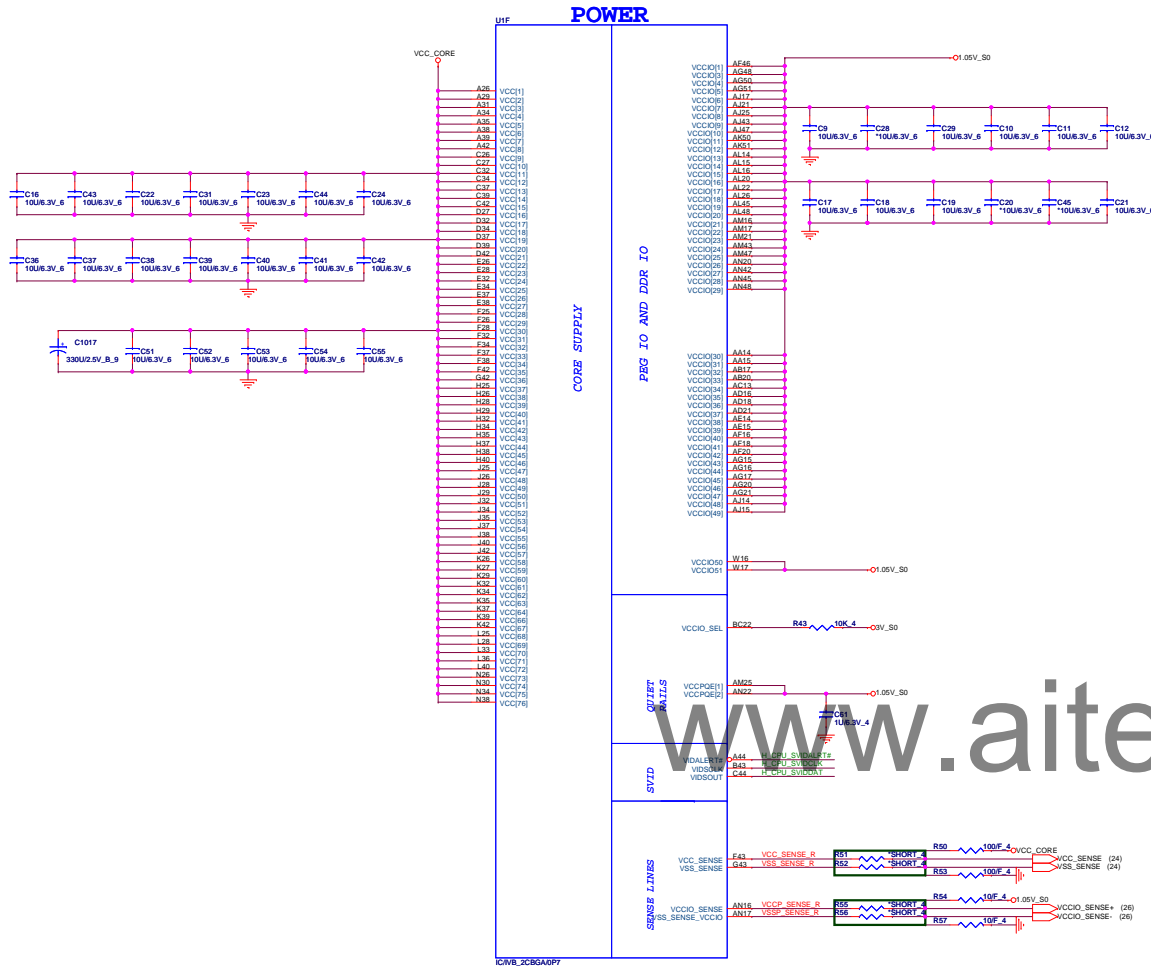


FAN Control-->For one FAN solution

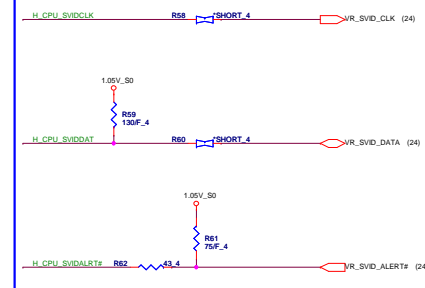


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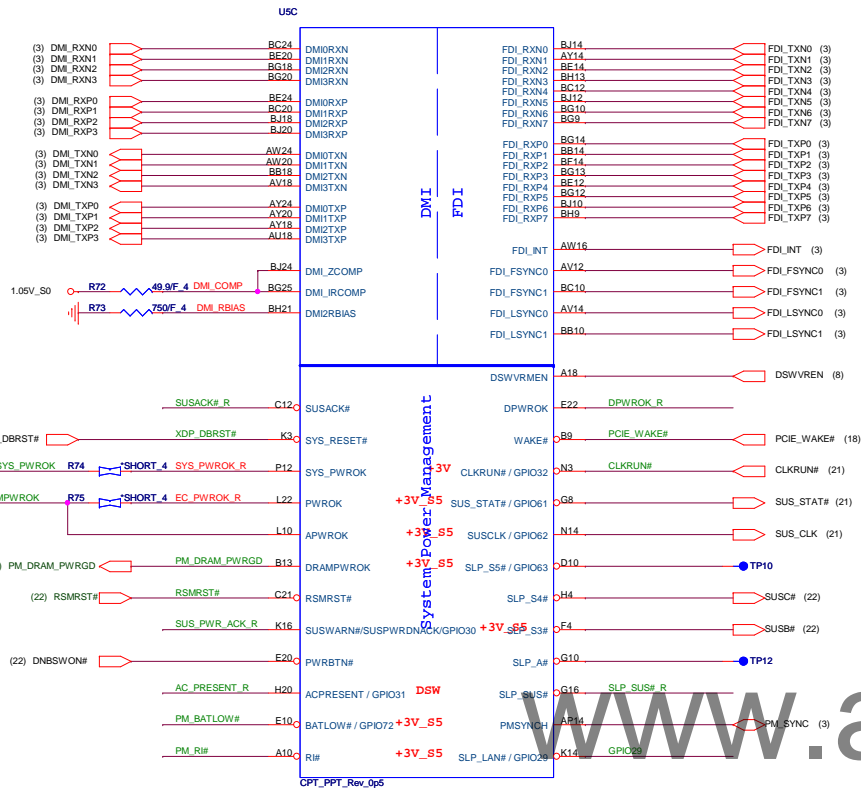
Layout note: need routing together and ALERT need between CLK and DATA



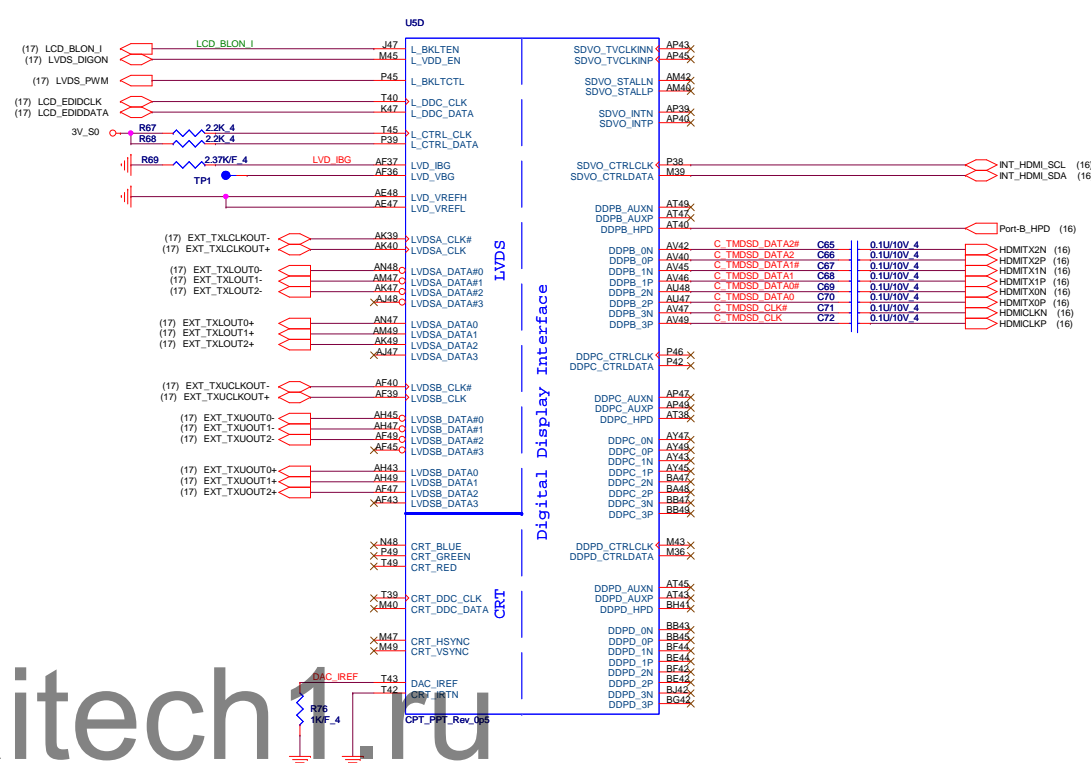


```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

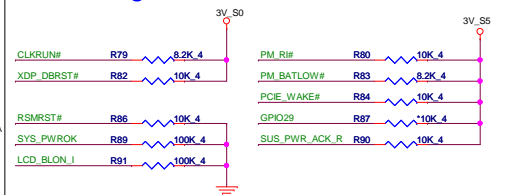
Panther Point (DMI,FDI,PM)



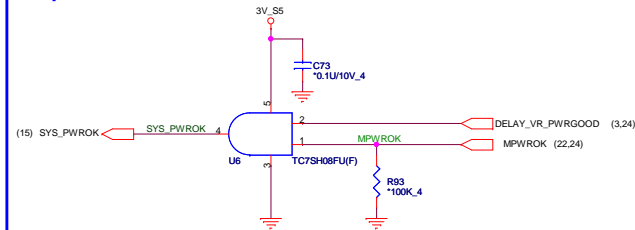
Panther Point (LVDS,DDI)



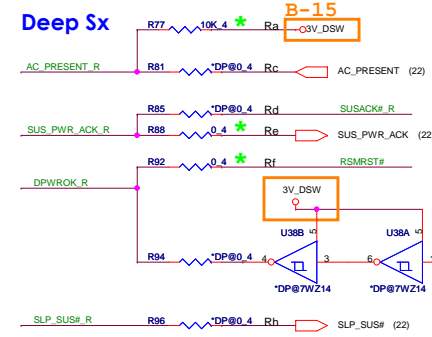
PCH Pull-high/low



System PWR_OK



Deep Sx



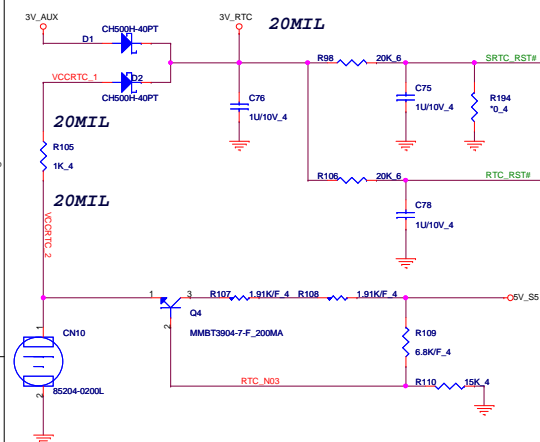
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff



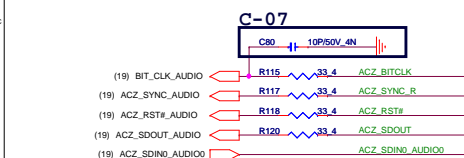
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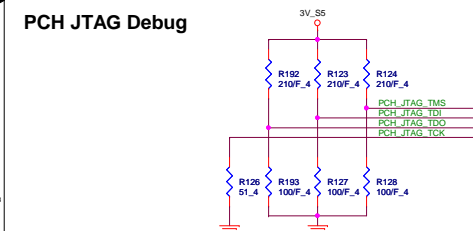
RTC Circuit



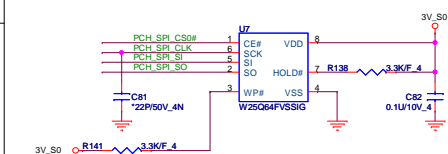
HDA Bus



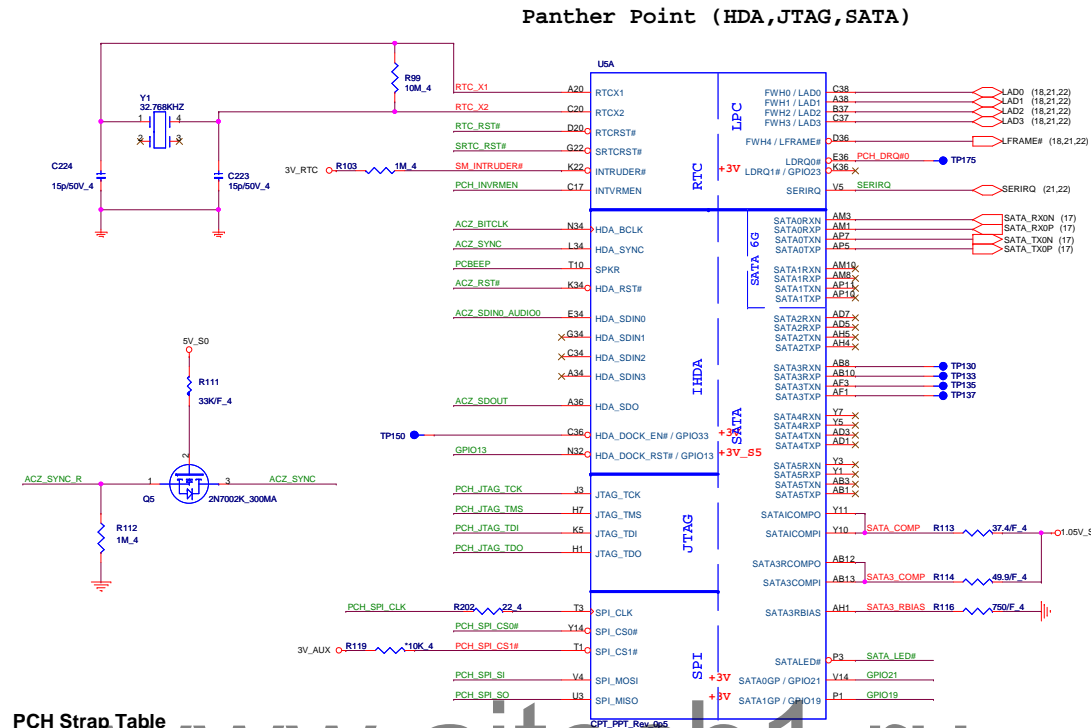
PCH JTAG Debug



PCH Dual SPI BIOS & ME F/W ROM 8MB



PCH2



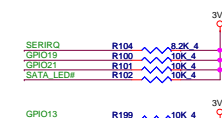
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0 ○ R121 *1K 4 POWER									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R122 *1K 4 PCI_GNT3# (9)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC ○ R125 *330K 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	R129 *1K 4 GNT1# (9) R130 *1K 4 GPIO19
GNT1#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Default (weak pull-down) 1 = Override	3V_S0 ○ R131 *1K 4 ACZ_SDOOUT ACZ_SDOOUT (22)									
DF_TVBS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R132 *22K 4 OT_8V_SFR DF_TVBS (10) R133 *1K 4 H_SNB_IVB#									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX ○ R134 *10K 4 PLL_OVDREN (1)									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 ○ R136 *1K 4 ACZ_SYNC									
GPIO15	TLS Confidentiality	RSMRST	0 = Default, TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 ○ R137 *1K 4 GPIO15 (10)									
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	3V_S5 ○ R139 *330K 4 DSWVRN (7) R140 *330K 4									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect									
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									

Panther Point (HDA,JTAG,SATA)

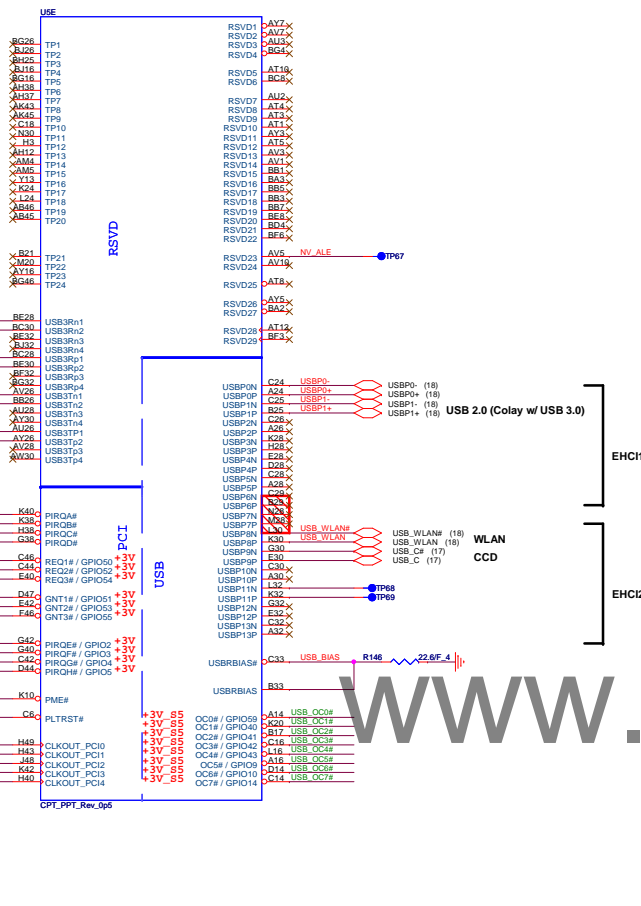
08

SATA SSD



Panther Point-M (PCI,USB,NVRAM)

Panther Point-M (PCI-E,SMBUS,CLK)



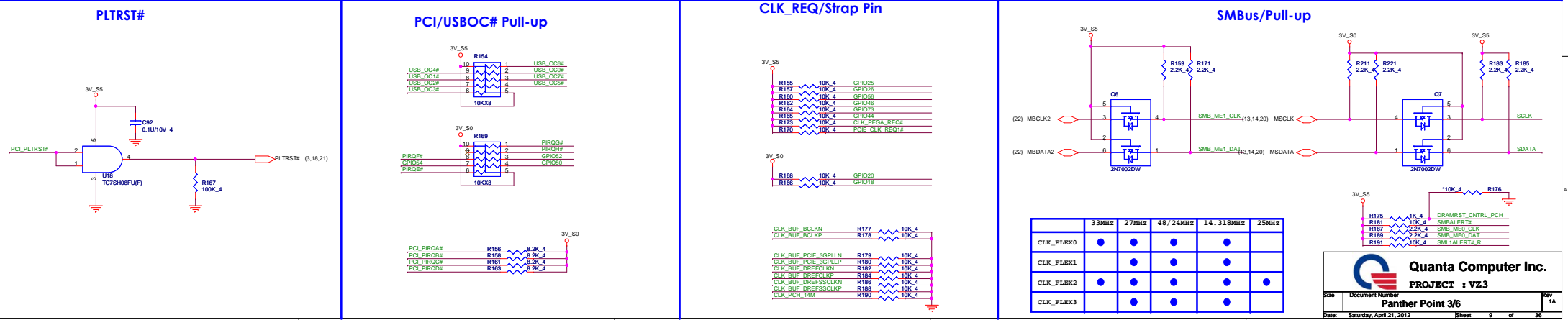
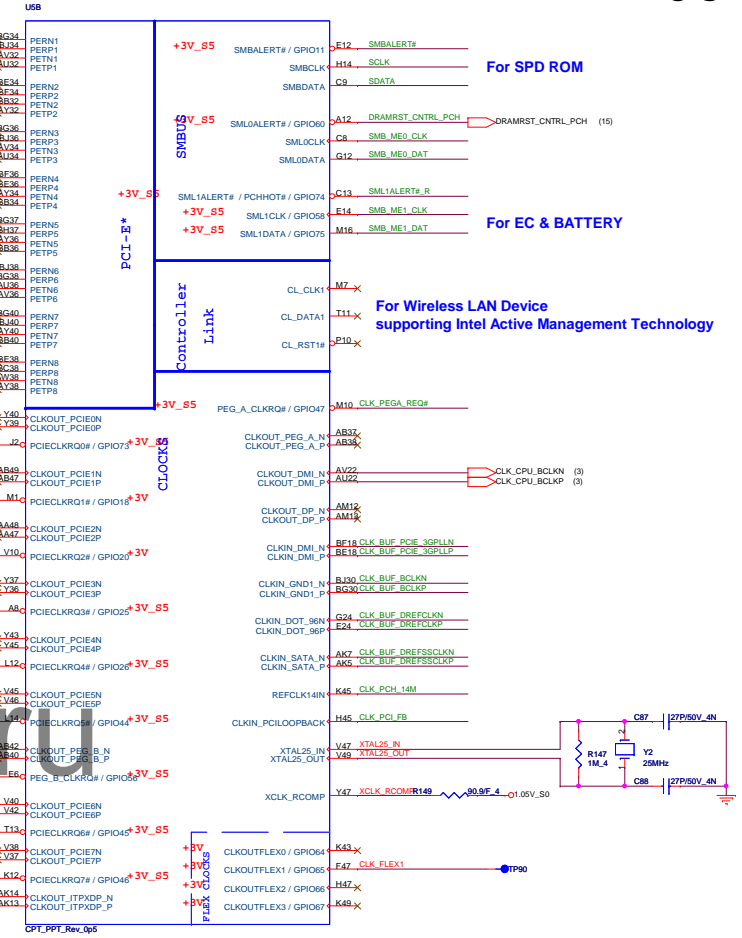
WLAN



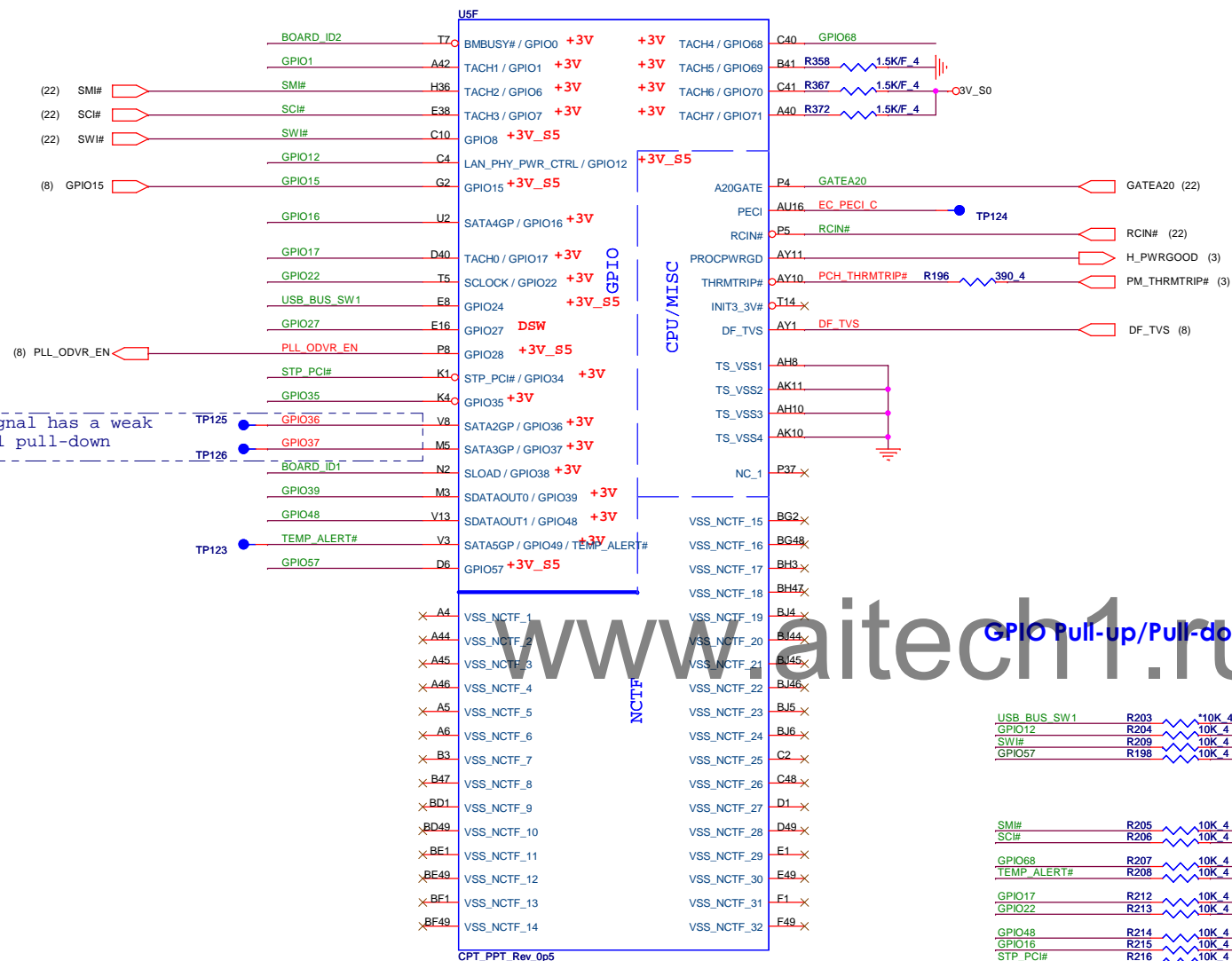
EHC1

EHC2

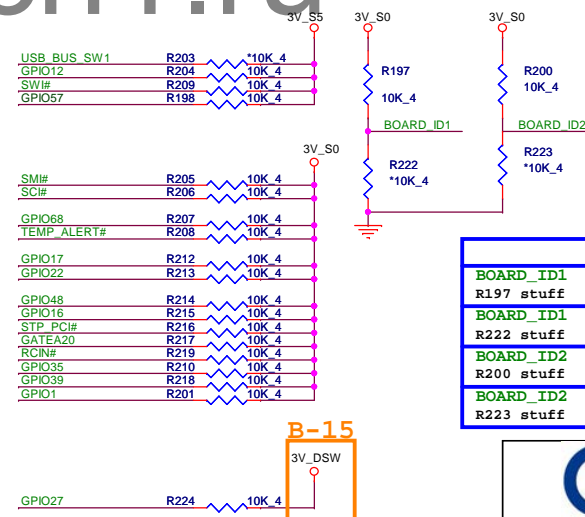
WLAN



Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down



	VZ1	VZ3
BOARD_ID1 R197 stuff	● (Hi)	
BOARD_ID1 R222 stuff		● (Lo)
BOARD_ID2 R200 stuff	● (Hi)	● (Hi)
BOARD_ID2 R223 stuff		

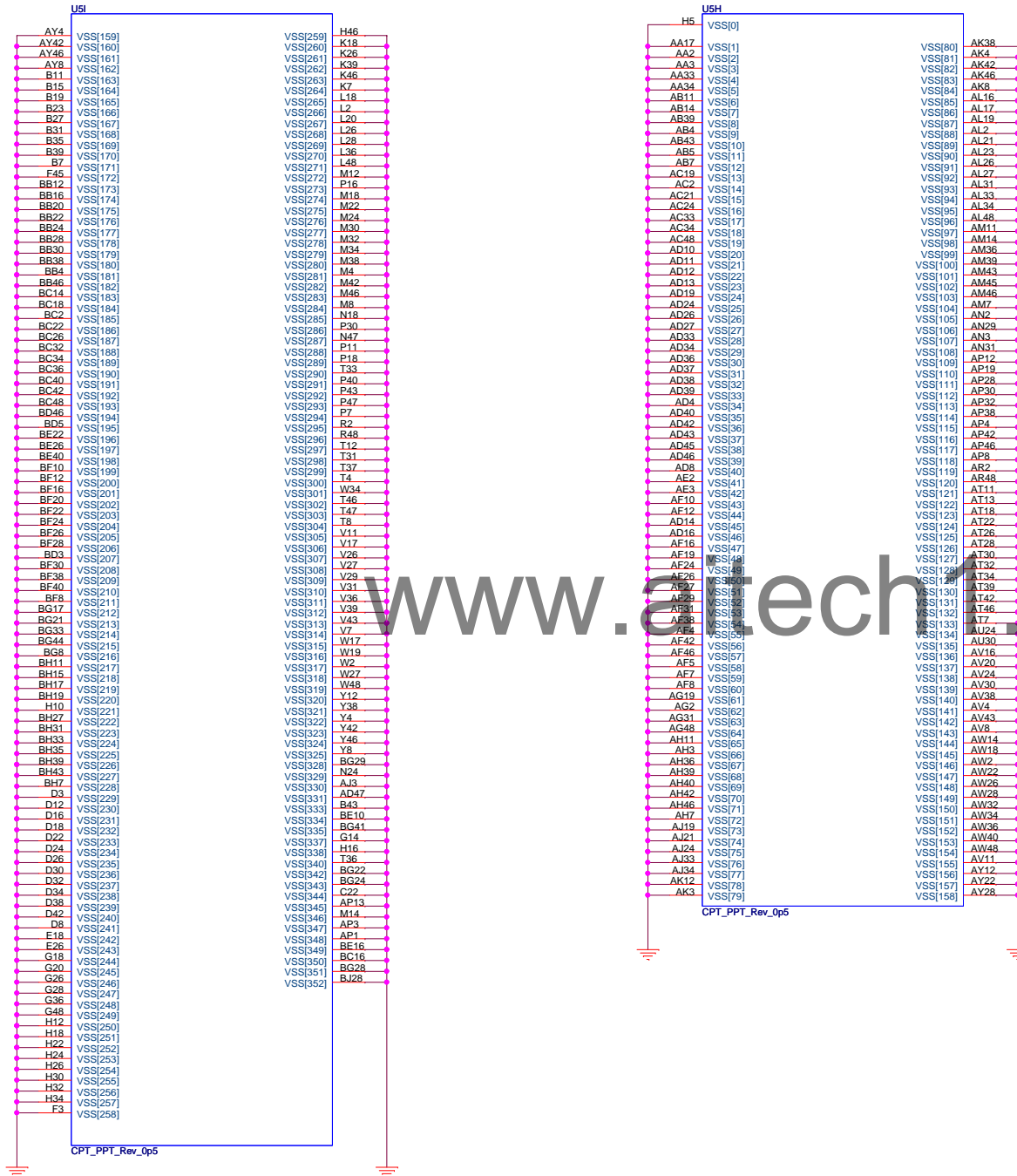


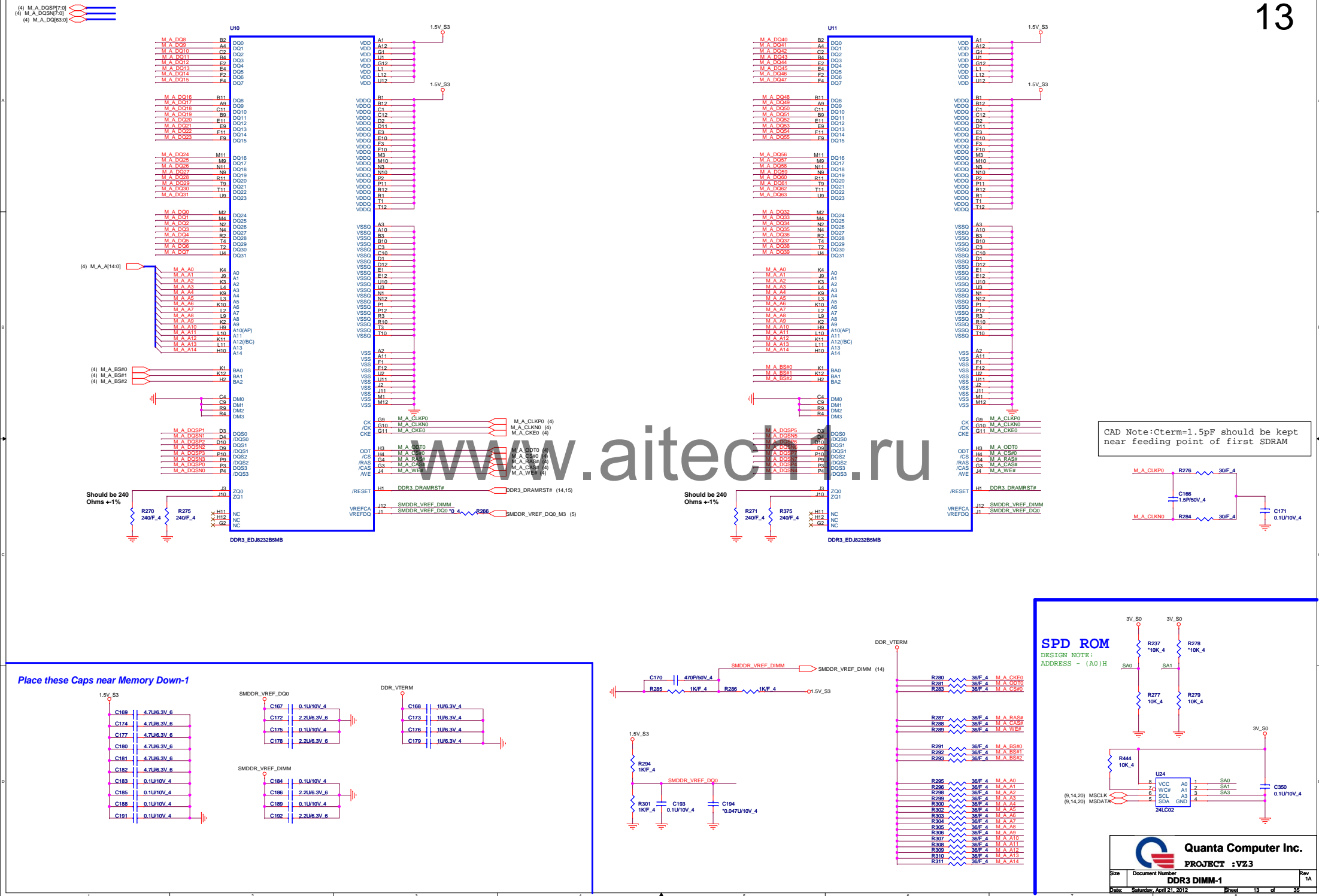
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Panther Point-M (POWER)







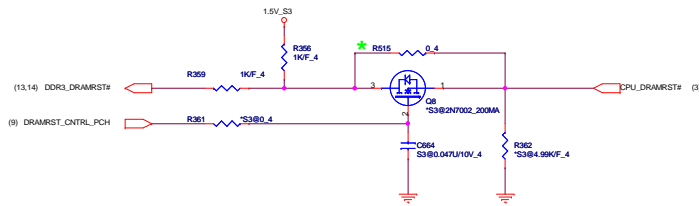


CAD Note:Cterm=1.5pF should be kept near feeding point of first SDRAM

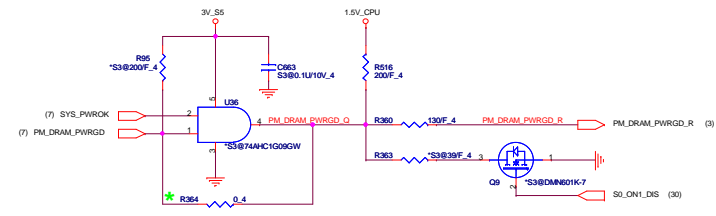


	DDR3 DIMM-2	1/
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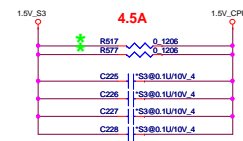
S3 power Reduction (SM_DRAMRST#)



S3 power Reduction (SM_DRAMPWROK)



S3 power Reduction (CPU Power)

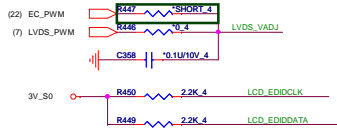
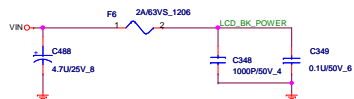
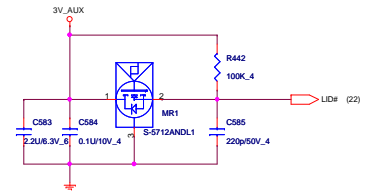
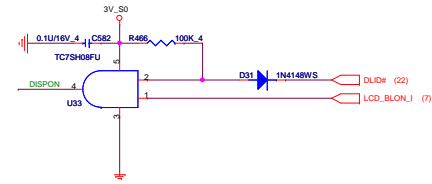
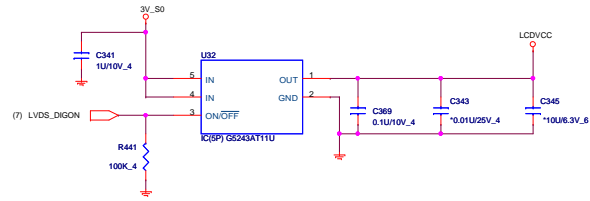
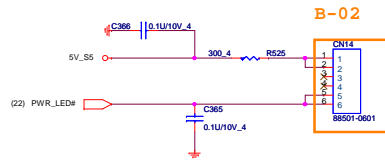


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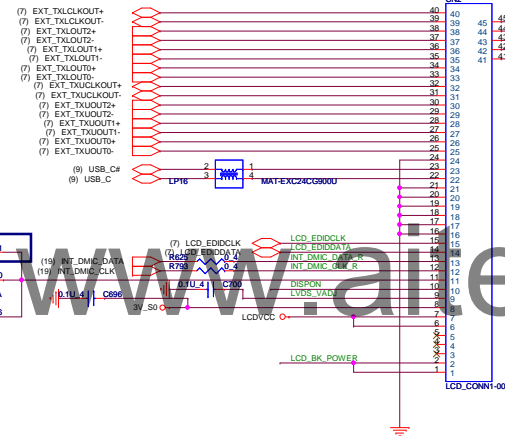
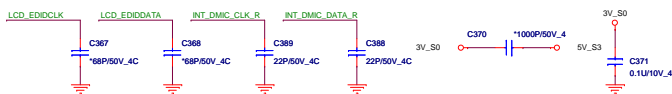


CFG = LOW: LOW-level input voltage: <0.40 V, LOW-level output voltage: 0.60 V
CFG = HIGH: LOW-level input voltage: <0.44 V, LOW-level output voltage: 0.66 V
HDMI_CFG1 = LOW: Passive DDC buffer
HDMI_CFG1 = HIGH: Active DDC buffer

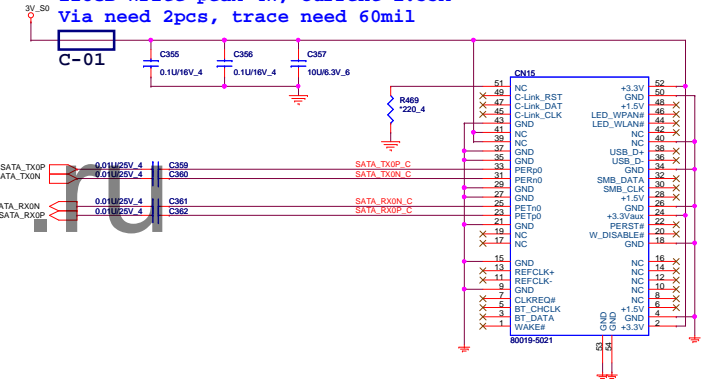
0.2A(20mils)



For EMI close to connector

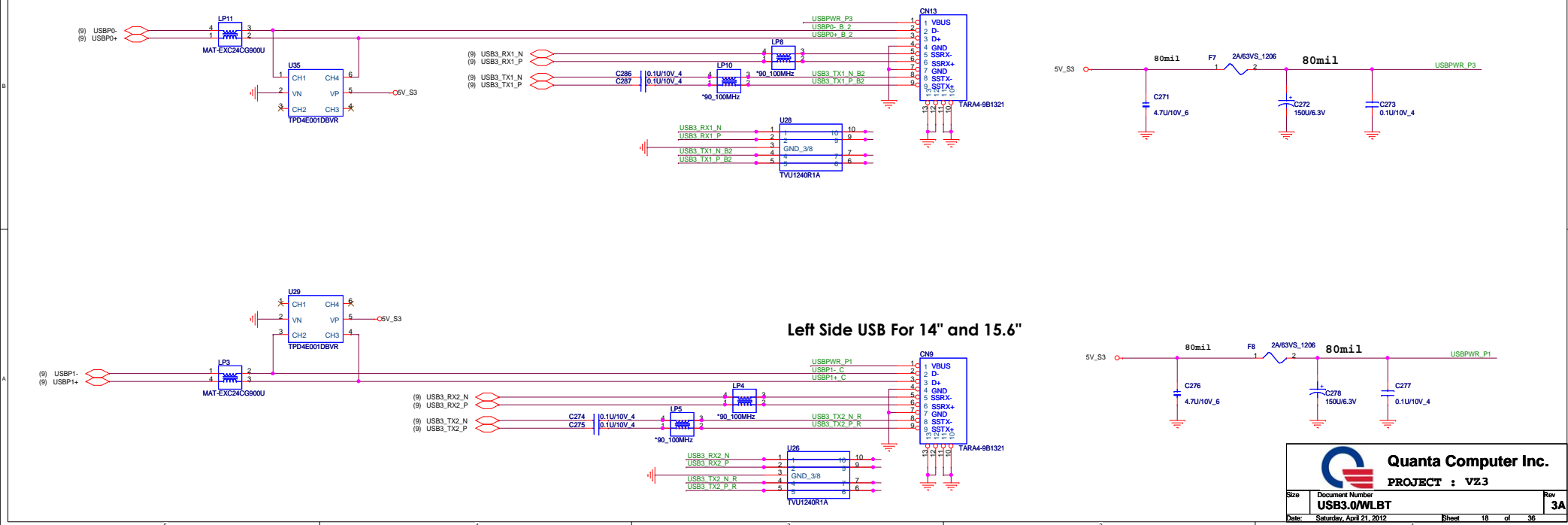


128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil

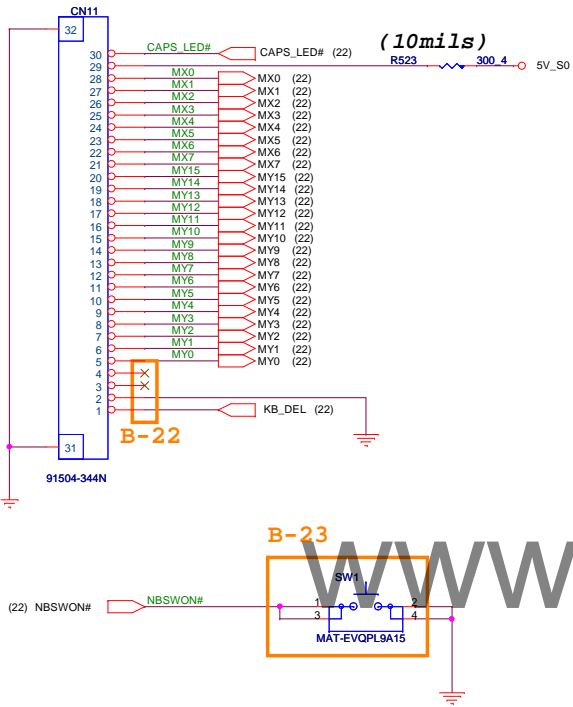




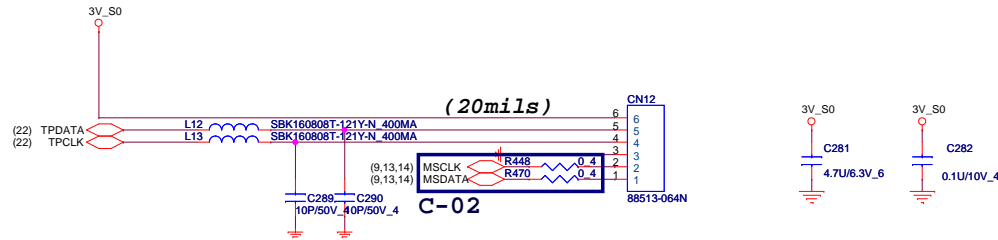
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INT KeyBoard



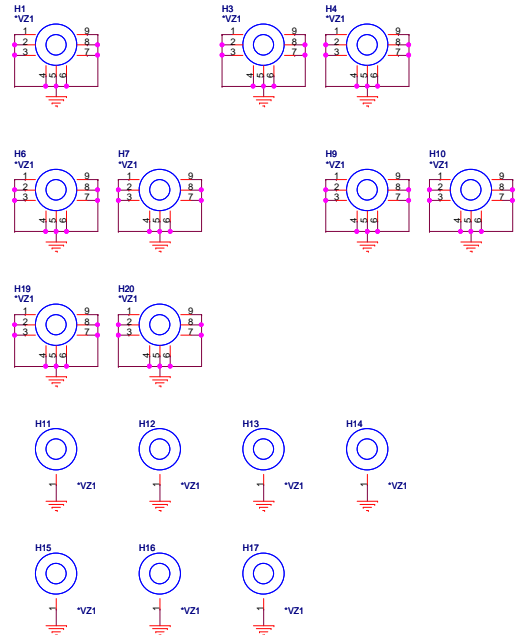
TP board



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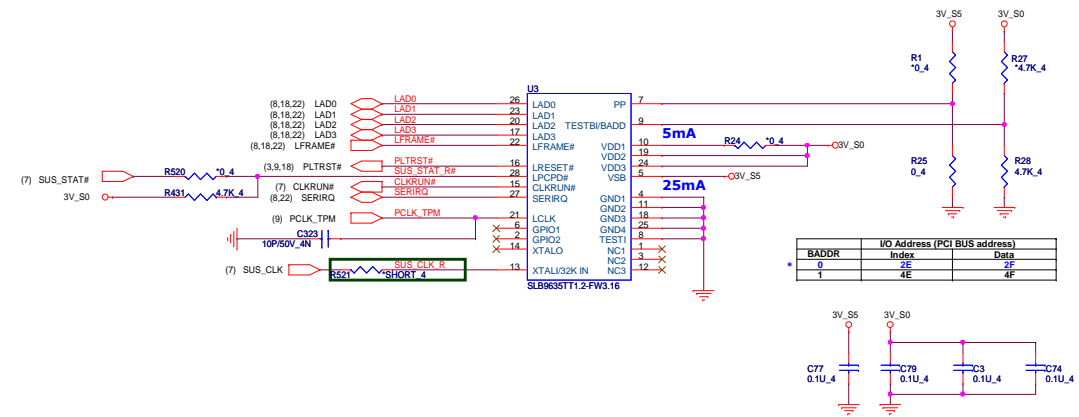
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HOLE

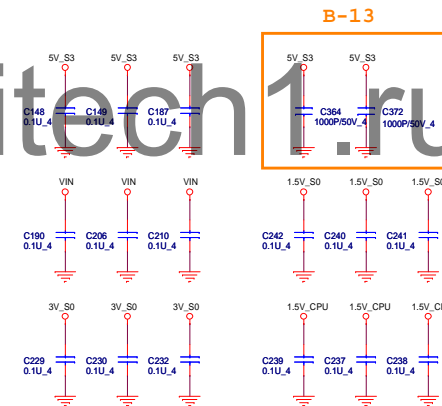


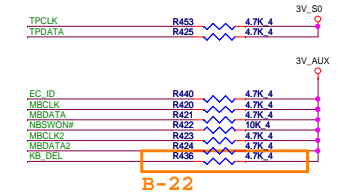
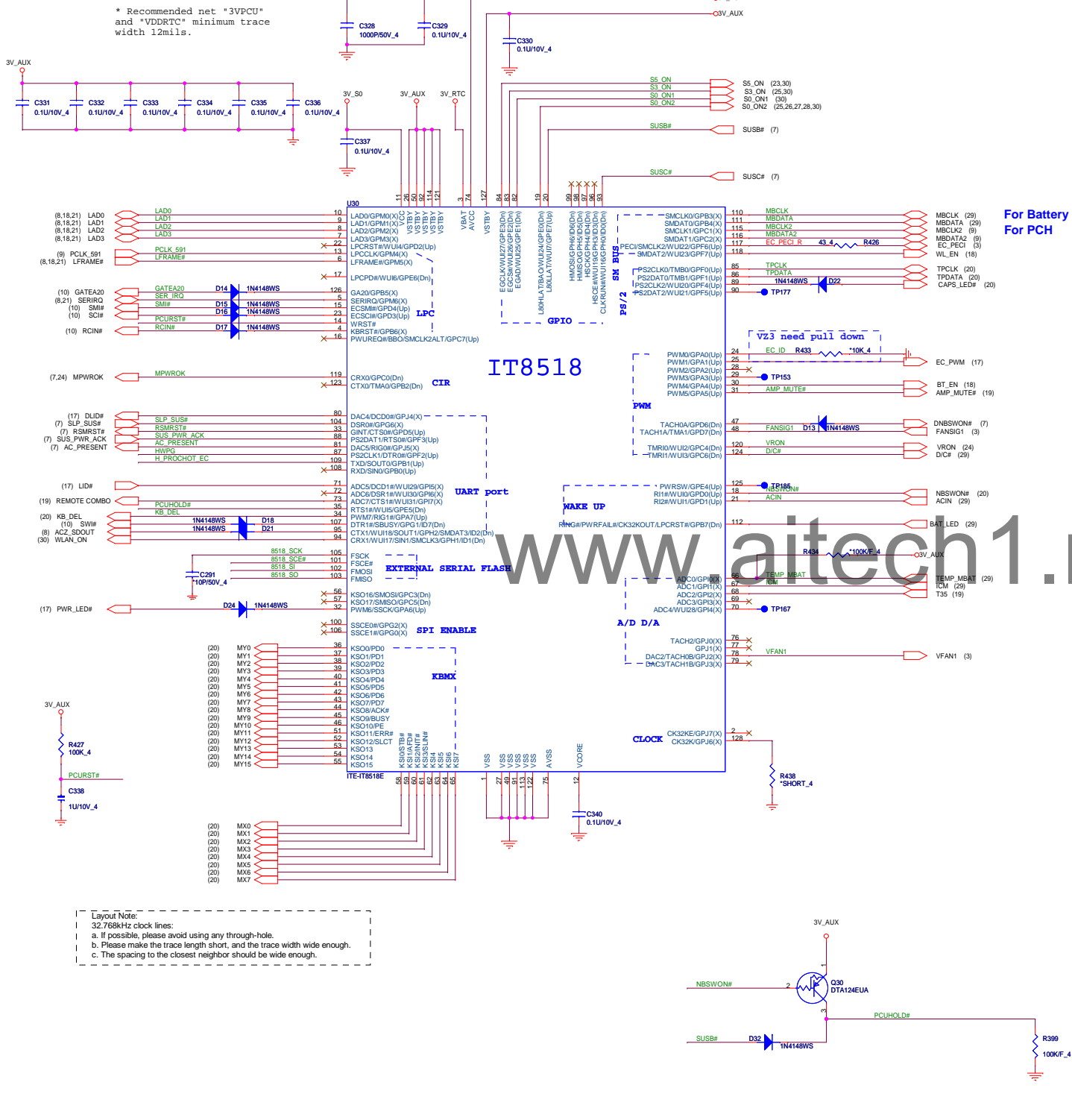
TPM

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EMI

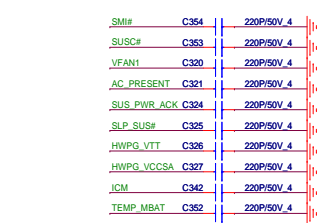




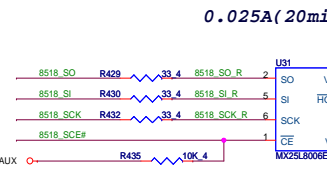
VZ1	R440	Hi
VZ3	R433	Lo

For Battery
For PCH

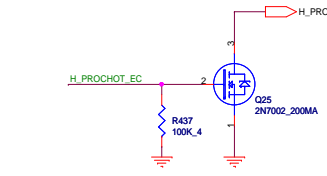
EMI



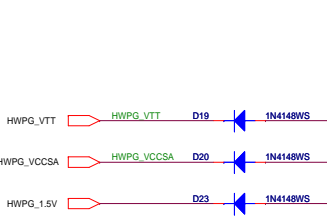
EC ROM 1MB

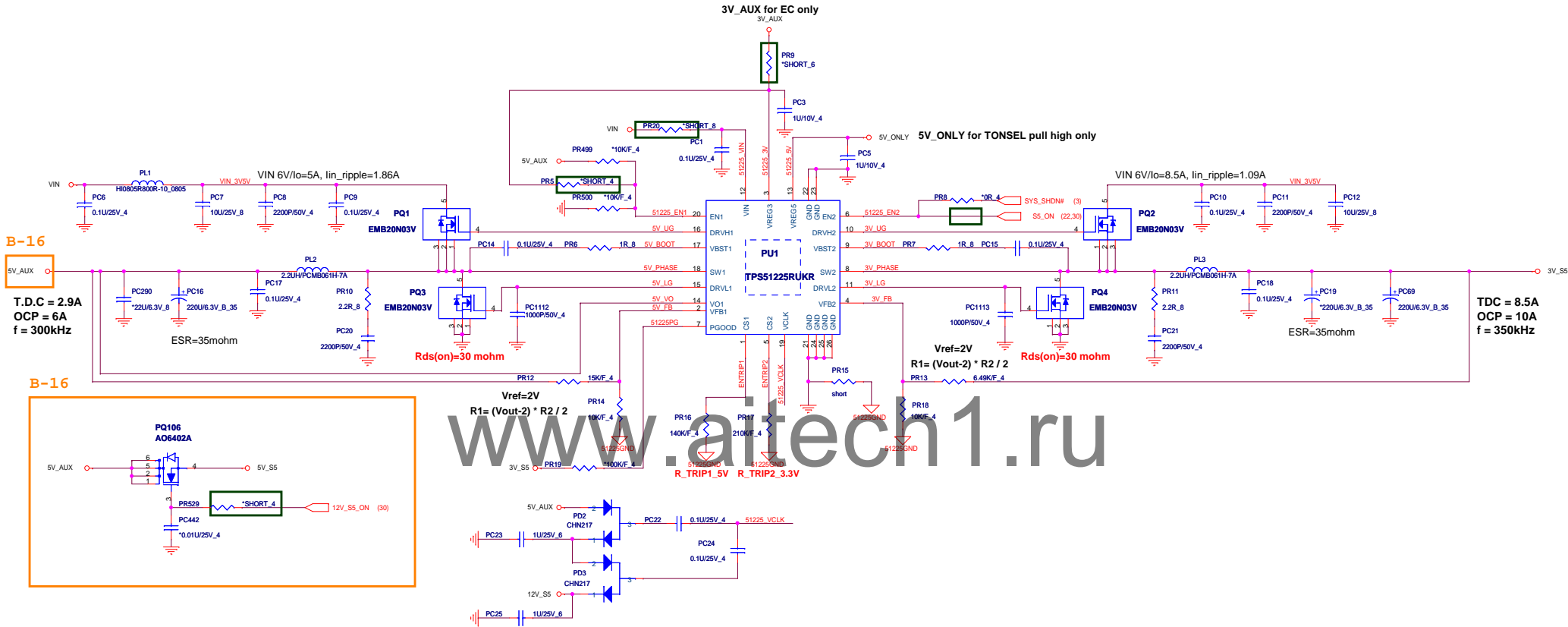


For throttling



HWPV circuit





$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	9	3.68	365	2.5uH	215K
3.3V	17.5m_Max	7.5	2.18	460	2.5uH	196K

L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
AP4438GM-HF	SO-8	11.8A	18m
EMB12N03G	SO-8	12A	15m
SI4134DY	SO-8	14A	17.5m
EMB20N03V	DFN3x3	12A	30m
MDV1525	DFN3x3	24A	14m
TPCC8065-H	DFN3x3	13A	14.5m

Power On sequencing


EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

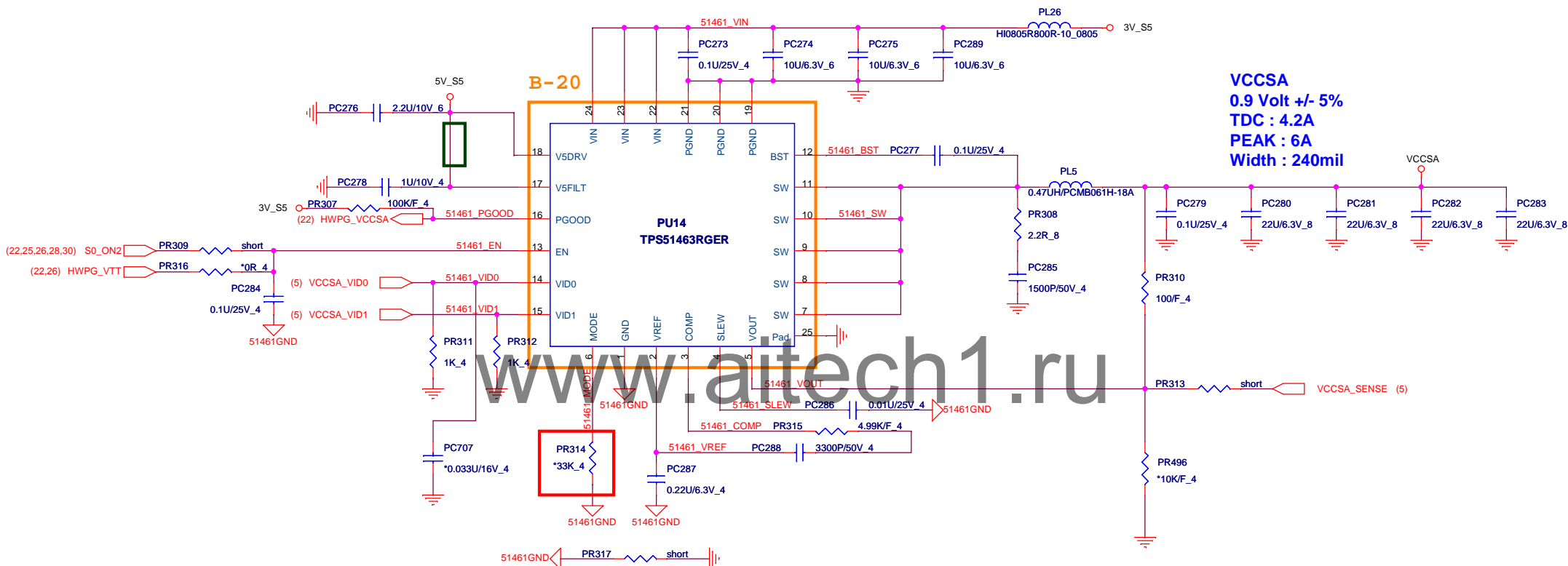


Output	Mos Rds_on	I_OCP	OC_AIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	12m_Max	10.5	2.3	400	1.5uH	11.5K

Mosfet	Package	ID (Ta=25C)	Rds_on_max
FDMC7692S	DFN 3*3	12.5A/18A	12m
AON7702	DFN 3*3	13.5A/20A	14m



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VCCSA PWM IC(PU14) Controller

CPU	Vendor P/N	QCI P/N	PR314	QCI P/N
Sandy Bridge	TPS51461RGER	AL051461000	33K	CS33302FB14
IVY Bridge	TPS51463RGER	AL051463000	NA	

IVY Bridge Table

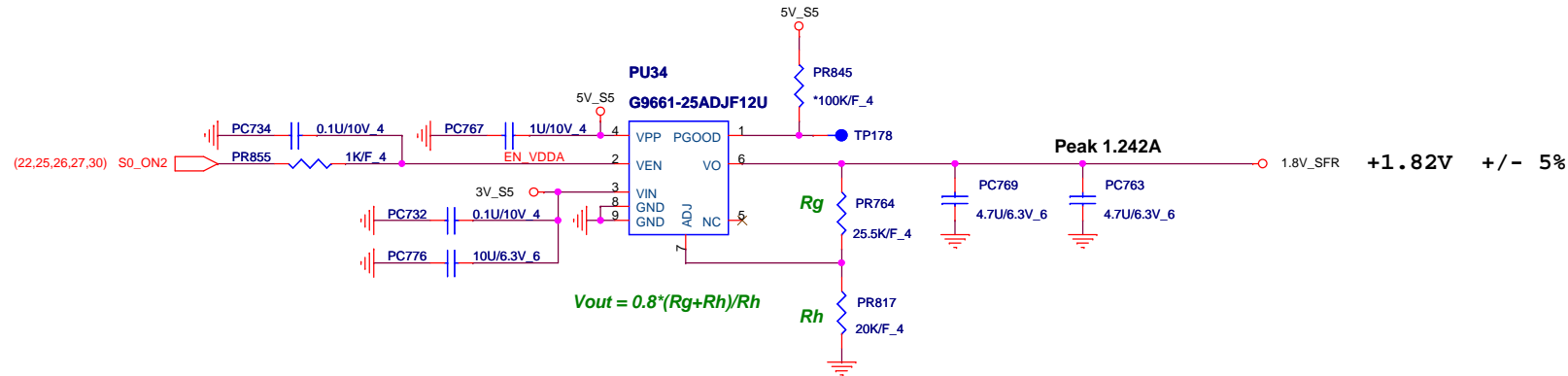
VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.750V

Sandy Bridge Table

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	Note
1	1	Note

1.8V_SFR (G9661-25ADJF12U)

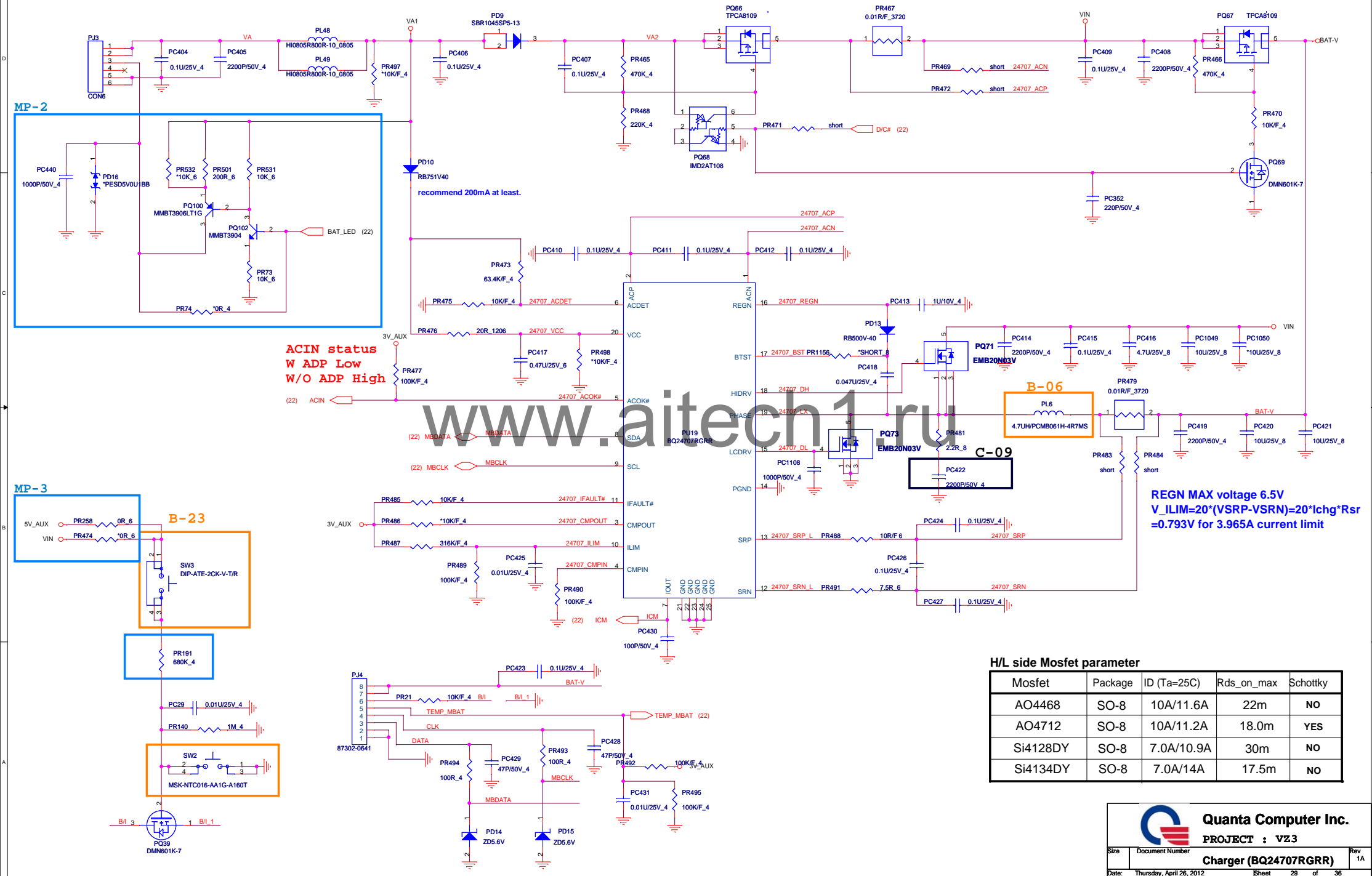
28



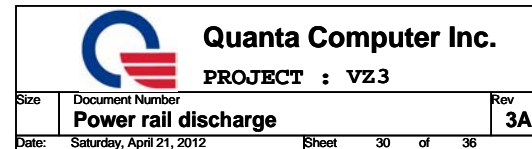
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Vga 10V, Id= 13A, Rds on 9m Max.,

Vga 10V, Id= 13A, Rds on 9m Max.,



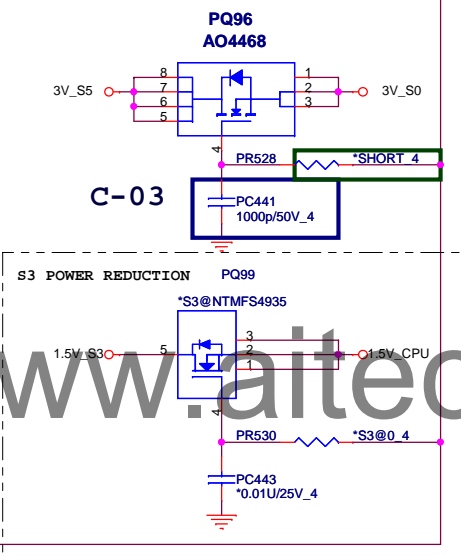
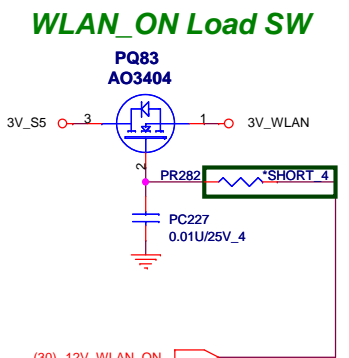
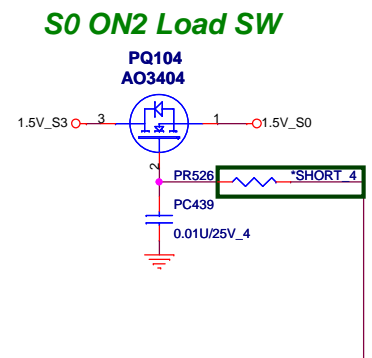
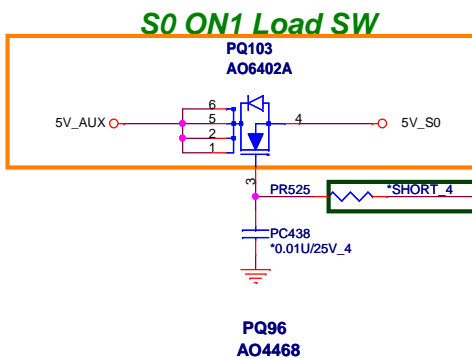
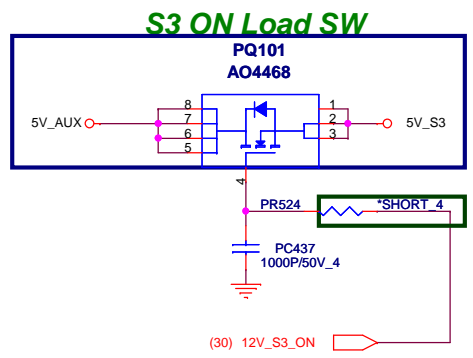
30



Load Switch

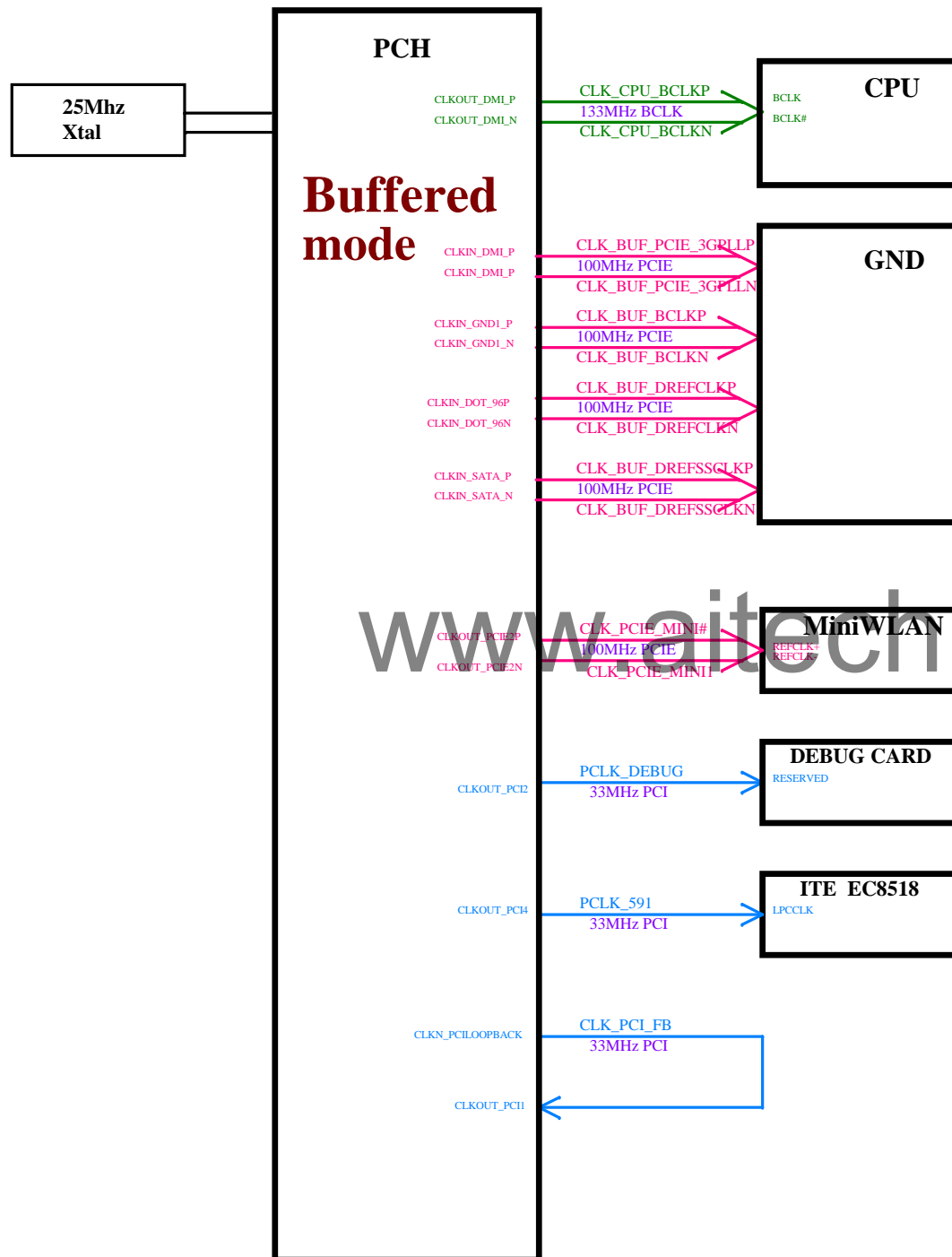
Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	10A/11.6A	22m	+/- 20V
AO4496	SO-8	7.5A/10.0A	26m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V

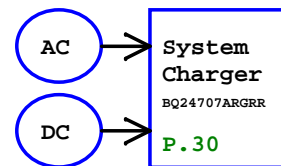


(30) 12V_S0_ON1

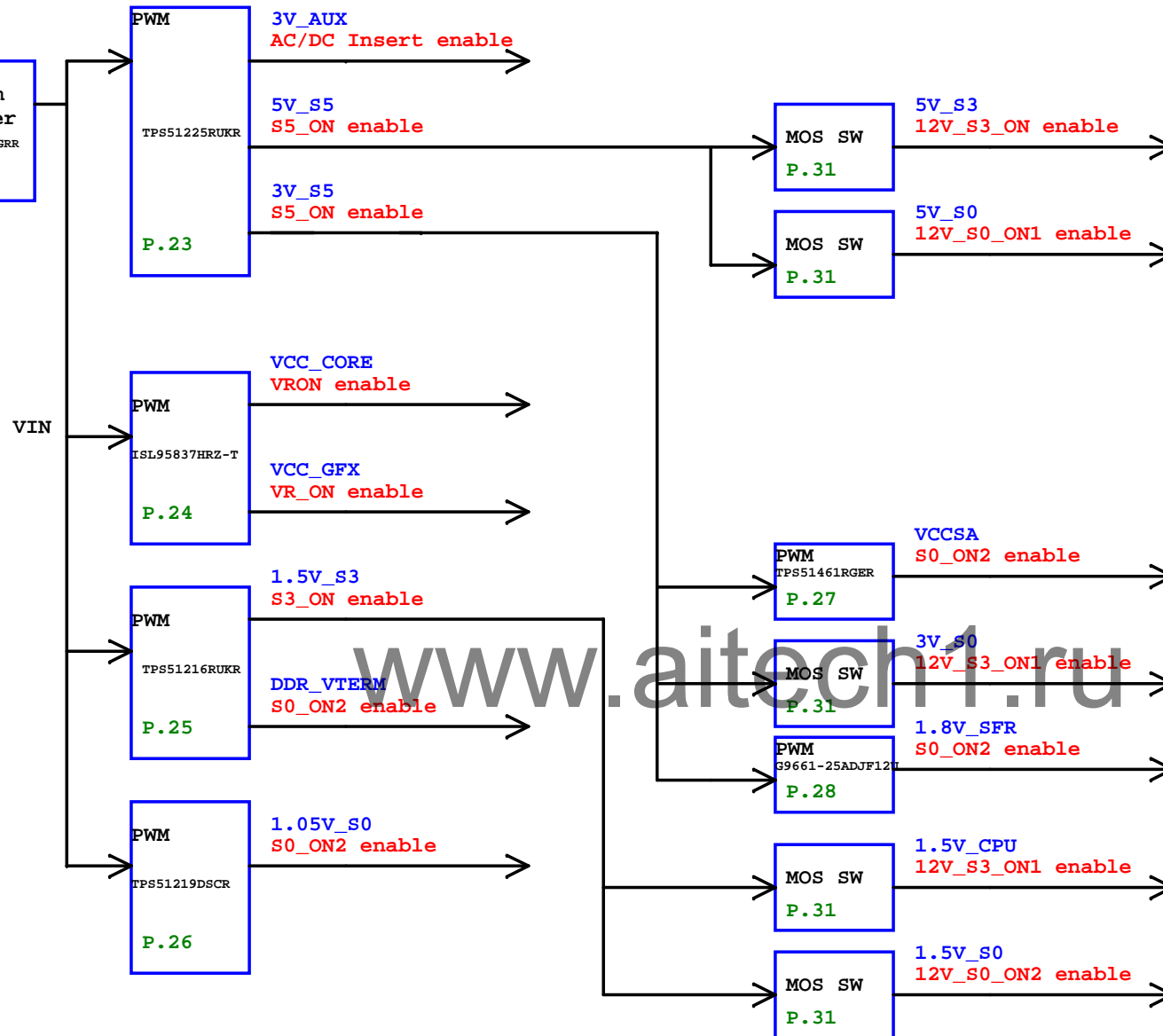
(30) 12V_S0_ON2



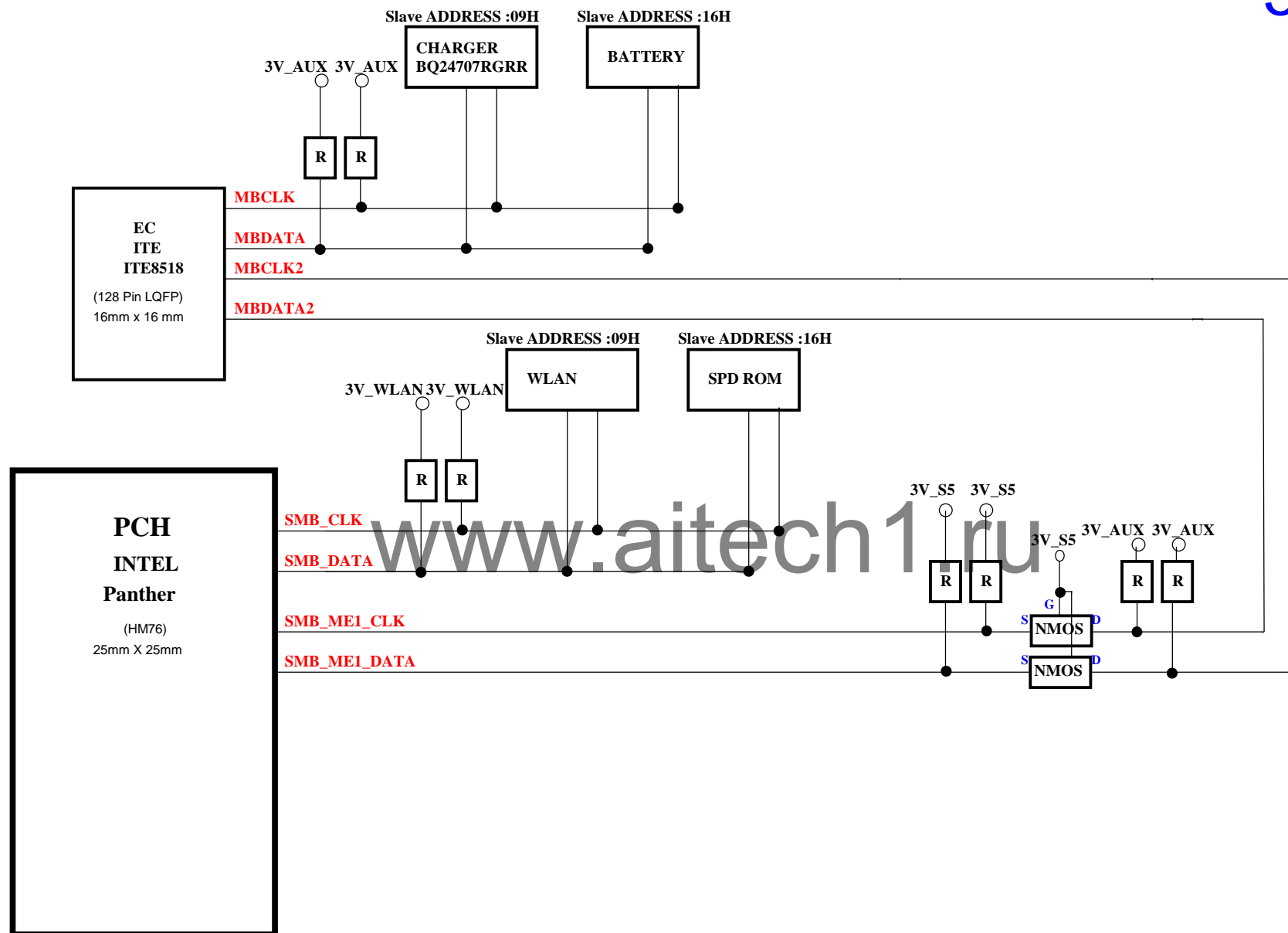
Power Tree Table



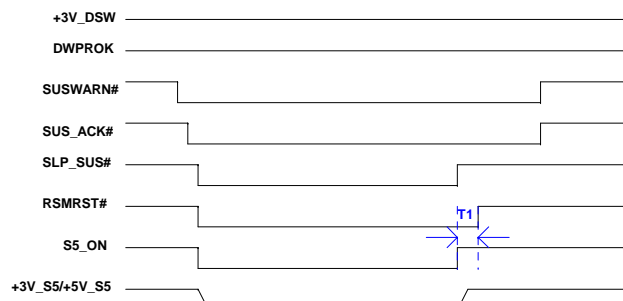
19V
3.42A



33



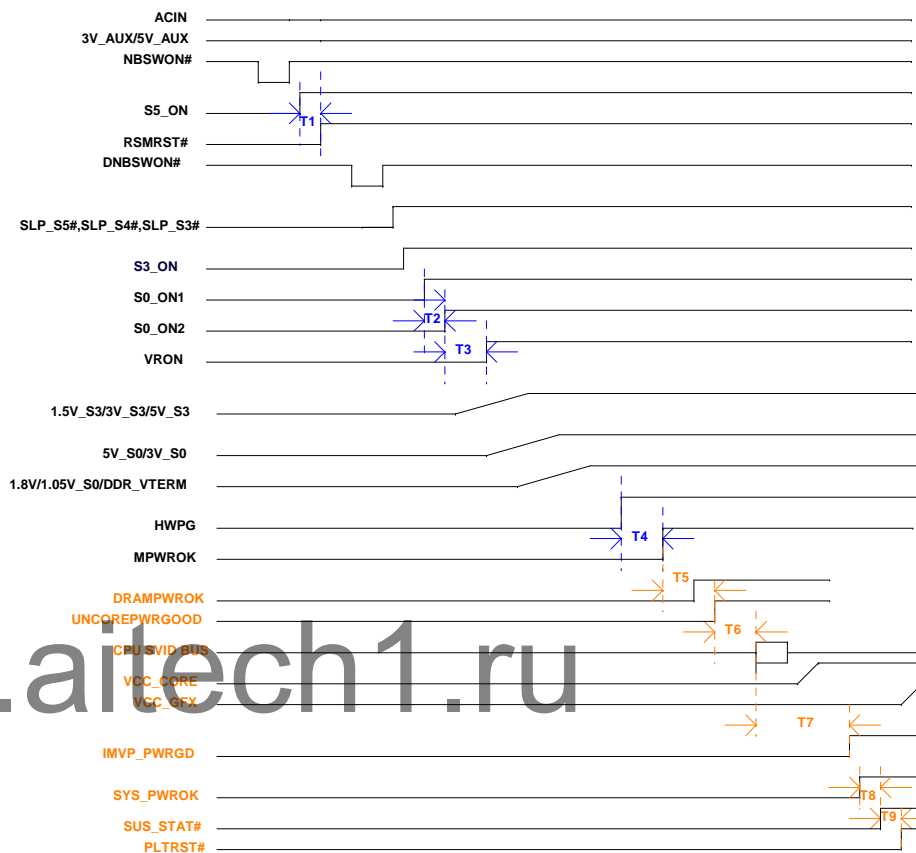
Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence

T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

System Power-ON Sequence



System Power Sequence

EC Control:

T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)

T2: S0_ON1 TO S0_ON2 = 500us

T3: S0_ON2 TO VRON = 10ms

T4: HWP TO MPWROK = 110ms (spec:mini 99ms)

Note: HWP NEED TO BE HIGH at that time

System:

T5: MPWROK to UNCOREPWROK = 2ms(Min)

T6: UNCOREPWROK to SVID Packet = 500us(Max)

T7: SVID Packet to IMVP_PWRGD = 5ms(Max)

T8: SYS_PWROK to SUS_STAT# = 1ms(Min)

T9: SUS_STAT# to PLTRST# = 60us(Min)

Model	REV	CHANGE LIST
VZ1 MB	B	B-01.Add EMI solution B-02.Change CN14 LED connector B-03.Add keyboard EMI solution B-04.Add AR16 pull high B-05.PR1127 CHANGE FROM 1.82K TO 1.87K,PR1122 CHANGE FROM 1.87K TO 1.78K,PR1108, PR1154 CHANGE FROM 6.98KTO 6.2K for VCC_CORE loline B-06.PL6 CHANGE FROM 6.8UH TO 4.7UH for charge current change to 0.5C. B-07.JS7 CHANGE TO SWITCH , PR474 CHANGE FROM 680K TO 1M,PC88 , PR20 DELETE B-08.PQ101& PQ103 CHANGE FROM A03404 TO A06402A,PC437 CHANGE FROM 2200P TO 1000P B-09.Del D6 for HDMI power issue B-10.NA AC37 , AC40 , ADD AC31,AC32,AC35,AC38 100P , AL5,AL6,AL7,AL8 CHANGE FROM 0OHM TO BEAD for SPK CIRCUIT. B-11.ADD U39 for TO EC ADC PIN B-12.ADD AL9 , AL10 bead for EMI . B-13.ADD C364 , C372, C1018, C1019, C1020, C1021 cap for EMI request B-14.Del PR181 SMDDR_VREF power source B-15.Change power source to 3V_DSW B-16.Add 5V_AUX switch MOSFET & Discharger B-17.add pc1051,pc1052,pc1053,pc1016,pc291,pc293 for cpu loline B-18.add 1.5V CPU Power rail discharge B-19.Change SW_VREF Power rail to 1.5V_CPU B-20.change from PR314 remove TPS51461RGER(AL051461000) to TPS51463RGER(AL051463000) B-21.PR1138 change from 2.37K(CS22372FB11) to 3.16K(CS23162FB04) B-22.Del R172,R504,C292 for KB remove POWER LED,Add R436 pull hi for KB_DEL B-23.Change POWER SWITCH SW1 to DHPPL9A1500,add SW2 & SW3
	C	C-01.Del R233 for cost down C-02.Add SMBus for touch pad vendor request C-03.Add PC441 to 1000P for SSD not found issue C-04.Change AO6402 to AO4468 for power noise issue C-05.Add PC440 for EMI request C-06.Change AL12 , AL13 to bead for EMI. C-07.Add C80 10P for EMI. C-08.Add AC1,AC2,AC3,AC5,AC11,AC12 to 1000P for EMI. C-09.Add PC422 to 2200P for EMI.
	MP-1	MP-1.add AU6(LMV331SN3T1G) , AR32(0OHM) , AR27(12K) , AR26(10K) , change AR66 to 6.8K . MP-2.Add PR532(10K) , PR501(10K) , PR531(10K) , PQ100(MMBT3906) , PQ102(MMBT3904) , PR73(10K) . MP-3.Add PR258(0OHM) , PR191(680K) , NA PR474(1M) . MP-4.Add D33 MP-5. change AJK1

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